REMARKS

Claims 34-37, 46 and 53-61 are pending in the present application. Claims 34, 53, 55, 57 and 61 have been amended.

Claim Rejections-35 U.S.C. 103

Claims 34, 37, 46, 53, 60 and 61 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Egawa reference (U.S. Patent No. 6,229,215) in view of the Buckley, III et al. reference (U.S. Patent No. 5,477,082). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 34 includes in combination a BGA (ball grid array) type semiconductor device "including a base plate, a first resin that seals a frontside surface of the base plate, and a plurality of bumps formed on a backside surface of the base plate that is opposite the frontside surface"; and a CSP (chip size packaged) type semiconductor device "mounted on an area of the backside surface of the base plate of said BGA type semiconductor device which does not have the plurality of bumps formed thereon". As further featured, "said CSP type semiconductor device has a second resin that covers the main surface of the semiconductor element and side surfaces of the terminals, the first and second resins are separate from each other". Applicants respectfully submit that the semiconductor device of claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

As noted above, a feature of the present invention is in a structure where a CSP type semiconductor device is mounted on a backside surface of a base plate of a BGA type semiconductor device. The frontside surface of the BGA type semiconductor device and the base plate are sealed by the first resin. The main surface of the semiconductor element of the CSP type semiconductor device and corresponding side surfaces of the terminals are sealed by the second resin, wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed and not covered. Moreover, the CSP type semiconductor device as mounted on the backside surface of the base plate has a thickness less than a thickness of the bumps by which the backside surface of the base plate is mounted on a printed circuit board. By employing such a structure, bad connections between the bumps and the printed circuit board on which the semiconductor device is mounted can be avoided or reduced. Moreover, as the side and back surfaces of the semiconductor element are not covered with resin, radiation of heat from the CSP type semiconductor device is not degraded, even if the CSP type semiconductor is mounted in narrow space.

Fig. 4 of the Egawa reference as primarily relied upon by the Examiner is descriptive of a process of making the semiconductor device as shown in Fig. 3. Although the side surfaces of second semiconductor chip 17 are not covered with resin in Fig. 4, it should be understood that Fig. 4 illustrates the structure at an intermediate processing step, not at a final state of the device as mounted on motherboard 50 as shown in Fig. 8 for example. In the final state of the device as mounted on

motherboard 50 shown in Fig. 8, second semiconductor chip 17 is entirely covered with resin 33. Figs. 1-3 of the Egawa reference incidentally also show side surfaces of second semiconductor chip 17 as covered by resin. Accordingly, the Egawa reference as relied upon by the Examiner does not disclose or suggest a semiconductor device including a CSP type semiconductor device having a semiconductor element with a back surface and an entirety of side surfaces exposed, whereby a base plate of a corresponding BGA device is mounted to a printed circuit board, as would be necessary to meet the features of claim 34.

Moreover, the structure as shown in connection with the processing step described with respect to Fig. 4 of the Egawa reference includes base plate 30 having through-hole 31 therein. Injected resin 33 reaches the surface of second semiconductor chip 17 by way of through-hole 31. Figs. 5 and 6 of the Egawa reference show side leak prevention jig 41 and air outlet ports 43 for preventing side leakage of resin between base plate 30 and second semiconductor chip 17. However, the final structure as mounted on motherboard 50 shown in Fig. 8 includes second semiconductor chip 17 enveloped by resin 33.

Furthermore, as should be readily understood in view of Figs. 5 and 6 of the Egawa reference, resin 33 seals the gap between first semiconductor chip 11 and base plate 30, and the gap between second semiconductor chip 17 and base plate 30, **in a single injection process**. That is, in Figs. 5-8 of the Egawa reference, the same resin seals both the front side surface of base plate 30 and the main surface of second

semiconductor chip 17. In contrast, a first resin seals a front side surface of the base plate in claim 34, and a second resin covers the main surface of the semiconductor element and corresponding side surfaces of the terminals, whereby the first and second resins are separate from each other. Clearly, the Egawa reference as primarily relied upon does not disclose these features.

On the other hand, the structure in the cover figure of the Buckley, III et al. reference includes carrier 60, with stiffener 62 and die 56 mounted on the front surface of carrier 60. Die 58 and solder balls 54 are mounted on the back surface of carrier 60. However, the cover figure of the Buckley, III et al. reference does not show dies 56 and 58 sealed by resin. More particularly, the Buckley, III et al. reference does not disclose first and second resins separate from each other, as would be necessary to meet the features of claim 34. The Buckley, III et al. reference thus does not overcome the above noted deficiencies of the primarily relied upon Egawa reference. Applicants therefore respectfully submit that the semiconductor device of claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 34, 37 and 46, is improper for at least these reasons.

The semiconductor device of claim 53 includes in combination among other features a BGA (ball grid array) type semiconductor device "including a base plate, a first resin that seals a frontside surface of the base plate, and a plurality of bumps formed on a backside surface of the base plate that is opposite the frontside surface";

and a CSP (chip size packaged) type semiconductor device "mounted on an area of the backside surface of the base plate of said BGA type semiconductor device which does not have the plurality of bumps formed thereon". As further featured, "the back surface and the entirety of the side surfaces of the semiconductor element are exposed, wherein the main surface of the semiconductor element is sealed with a second resin, and portions of each of the plurality of terminals are exposed from the second resin, the first and second resins are separate from each other".

Applicants respectfully submit that the prior art as relied upon by the Examiner does not make obvious the above noted features. As emphasized previously, the final structure as shown in Fig. 8 of the Egawa reference including the semiconductor device mounted on motherboard 50 has second semiconductor chip 17 enveloped by resin 33. Moreover, first and second resins separate from each other are not disclosed. The Buckley, III et al. reference does not overcome these deficiencies. Accordingly, Applicants respectfully submit that the semiconductor device of claim 53 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 53, 60 and 61, is improper for at least these reasons.

Claims 35, 36 and 54-56 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Egawa and Buckley, III et al. references, in further view of the Lin et al. reference (U.S. Patent No. 5,239,198). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

Applicants respectfully submit that the Lin et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the primarily relied upon prior art. Passive electronic component 50 as shown in Figs. 6 and 7 of the Lin et al. reference is not specifically described as a CSP (chip size packaged) type semiconductor device. Moreover, passive electronic component 50 is not specifically described or shown as having a main surface sealed with a second resin, wherein portions of each of a plurality of terminals are exposed from the second resin. Accordingly, Applicants respectfully submit that claims 35, 36 and 54-56 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of three (3) months to November 14, 2008, for the period in which to file a response to the outstanding Office Action. The required fee of $1110.00

should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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